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IN THE UNITED STATES PATENT & TRADEMARK OFFICE

IN RE APPLICATION OF : DATE ALLOWED: NOVEMBER 7, 2005
RYU OGAWA, ET AL. : EXAMINER: MAI, S.
SERIAL NO: 10/830,046 :
FILED: APRIL 23, 2004 : GROUP ART UNIT: 2827
FOR: SEMICONDUCTOR INTEGRATED :
CIRCUIT DEVICE

COMMENTS ON STATEMENT OF REASONS FOR ALLOWANCE

COMMISSIONER FOR PATENTS
ALEXANDRIA, VIRGINIA 22313

SIR:

Applicant acknowledges with appreciation the indication of allowability of the claimed invention. In response to the Examiner's Statement of Reason for Allowance in the Notice of Allowance of November 7, 2005, Applicant respectfully submits the following comments.

In the Examiner's Statement of Reasons for Allowance on page 2 of the Notice of Allowance mailed November 7, 2005, paragraph 2 states:

The following is an examiner's statement of reasons for allowance: The prior art of record fails to teach or suggest a semiconductor integrated circuit device comprising: a memory cell array including a memory cell having a ferroelectric capacitor, the memory cell having a first electrode; a second bit line complementary to the first bit line; a first potential generation circuit which supplies a first potential to the second electrode to apply a voltage dropping at a first rate of change with a rise of temperature to the ferroelectric capacitor, the first rate of change being equal to dependence on temperature possessed by a saturate voltage of the ferroelectric capacitor.

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However, it is respectfully noted that independent Claims 5, 6, 16, and 18 do not include all of the elements recited in paragraph 2 of the Notice of Allowance. Accordingly, it is respectfully submitted that the above-quoted statement applies only to Claim 1 and not to any of independent Claims 5, 6, 16, or 18.

Respectfully submitted,

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